INDEX SHEET

#	Subject code	Subject	Faculty Handling
1	UE19EC301	Computer Communication Networks	**Prof.M Rajasekar**, Prof.Prajeesha, Prof.Veena S, Prof.Shruthi S V
2	UE19EC302	Digital VLSI design	Prof.S S Rekha, Prof.Annapurna K Y, Prof.Hema N Prof.Shruthi M L J **ECC: Dr. Shashidhar Tantry** Prof.Mahesh A
3	UE19EC303	Control systems	Dr.Anuradha M, Dr.Shikha Tripathi, **Prof.Karpagavalli S**, Prof.Rajini M, Prof.Thippeswamy ECC: Dr. Sireesha B Prof.Prahlad D
4	UE19EC304	Computer Communication Networks Laboratory	**Prof. M Rajasekar**
5	UE19EC305	Digital VLSI design Laboratory	**Prof.S S Rekha**
Elective - I			
6	UE19EC311	Information Theory and Coding	**Dr. Arpita Thakre**
7	UE19EC313	Advanced Digital Design	**Dr.Sudeendra Kumar K**
8	UE19EC316	Electronic Design Automation- Verilog to Routing	**Dr.Madhura Purnaprajna**
9	UE19EC317	Digital Image Processing	**Dr. Shikha Tripathi** ECC:Dr. Subhash Kulkarni
10	UE19EC318	Pattern Classification	**Dr. Manikandan J**
Elective - II			
10	UE19EC321	Wireless Communication	**Prof.Bharathi V K** ECC:Prof. Renuka R Kajur
11	UE19IE301	Operations Research	**Prof.Nagaraj L J**
12	UE19EC323	Real Time Operating Systems	**ECC:Prof.Bivas Bhattacharya** Prof.Y J Pavithra
13	UE19EC327	Artificial Neural Networks	**Prof.Swetha R**

COMPUTER COMMUNICATION NETWORKS (4-0-0-0-4)

Subject Code: UE19EC301 **No. of Hours: 56**

Faculty: Prof. MR/PR/VS/SSV

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 1 – Introduction				
1	1.2 (Textbook 1)	Introduction and Network edge	1.8	**18**
2	1.3	Network core	1.8	
3	1.4	Performance parameters	1.8	
4	1.5 and 2.1	Concept of layer-based communication. Windows commands (ping, tracert, network commands (windows), ipconfig etc)	1.8	
5	2.2.1 – 2.2.3	Web and HTTP, cookies	1.8	
6	2.3	Electronic email in the internet; Telnet	1.8	
7	2.4	DNS - The backbone of internet	1.8	
8	2.5 and 2.6.3	Content distribution CDN and PTP	1.8	
9	Chapter 1	Delay analysis – Web-caching, Numerical problems: Packet switching end-to-end delay, queuing delay; animation demo	1.8	
10	Chapter 1	Delay analysis (using approximate timing diagrams): HTTP problems DNS problems P2P problems; animation demo; /displaydns, ~/flushdns commands	1.8	
Unit 2 -Transport layer				
11	3.1 - 3.2	Transport layer introduction	1.83	**40**
12	2.7	Socket programming	1.83	
13	3.3	Connectionless transport	1.83	
14	3.4.1	Principles of reliable data transfer – Stop and wait protocols	1.83	
15	3.4.2 – 3.4.4	Principles of reliable data transfer – Pipelining	1.83	
16	3.5	TCP Reliable data transfer – Part 1	1.83	
17	3.5	TCP reliable data transfer – Part 2	1.83	
18	3.5	TCP reliable data transfer – Part 3	1.83	
19	3.7	TCP congestion control	1.83	
20	Chapter 2	Numerical problems: TCP Reliable data transfer	1.83	
21-22	Chapter 2	Numerical problems: Congestion control	3.66	

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 3 - Network Layer				
23	4.2.1 – 4.2.4	Internal organization of router; Functions of router	1.83	**62**
24	4.3.1 – 4.3.2	IPv4 datagram format and datagram fragmentation	1.83	
25	4.3.3	IPv4 Addressing: CIDR, sub-netting and super-netting	1.83	
26	4.3.3 and 5.6	DHCP and ICMP	1.83	
27	4.3.4	NAT, NAT Traversal, UPnP	1.83	
28	4.3.5	IPv6: Datagram format, Transitioning from IPv4 to IPv6	1.83	
29	5.2.1	Routing algorithms: Dijkstra algorithm	1.83	
30	5.2.2 (Textbook 1)	Routing algorithms: Bellman-Ford Algorithm	1.83	
31	4.6.1 – Textbook 2	Intra-AS routing protocol: Concept of Autonomous Systems, RIP	1.83	
32	5.3 and Reference 3	Intra-AS routing protocol: OSPF (Concept of Areas, Types of LSAs and Types of Packets)	1.83	
33	5.4.1 – 5.4.2	Inter-AS routing protocols (BGP): The Role of BGP, Advertising BGP Route Information	1.83	
34	5.4.3 – 5.4.5	Inter-AS routing protocols (BGP): Determining the Best Routes, IP Anycast, Routing policy	1.83	
Unit 4 - Link Layer				
35	6.1	Role and importance of link layer	1.83	**84**
36	6.2	Error detection techniques	1.83	
37	6.3.2	Basic random-access techniques	1.83	
38	6.4.1	Switched Local Area Networks	1.83	
39	6.4.2	Ethernet: protocol and frame format, Ethernet flavours	1.83	
40	6.4.3	Link layer switches: Forwarding	1.83	
41	6.4.4	Virtual Local Area Networking	1.83	
42-43	Chapter 6	Numerical problems	3.66	
44	7.3.1	IEEE 802.11: Architecture	1.83	
45	7.3.2	IEEE 802.11 MAC protocol	1.83	
46	7.3.3	IEEE 802.11 Frame and numerical problems	1.83	

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 5 –Miscellaneous/Advanced topics				
47	4.7.1 – Textbook 2	Broadcast algorithms	1.6	**100**
48	4.7.2 – Textbook 2	Multicast algorithms	1.6	
49	Reference 4	Point-to-point protocol (PPP)	1.6	
50	6.5	Multi-Protocol Label Switching	1.6	
51	4.1	Forwarding and Routing: Traditional versus SDN approach	1.6	
52	4.4	Generalized forwarding and SDN	1.6	
53	5.1 and 5.5.1	SDN Control Plane	1.6	
54	5.5.2	Open flow protocol	1.6	
55	8.1	Network security - overview	1.6	
56	8.7	Network Layer security	1.6	

Book Type	Author & Title	Publication information		
		Edition	Publisher	Year
Text book 1	JamesFKuroseandKeithWRoss ComputerNetworking:ATopDownApproach	Seventh	Pearson Education	2016
Text Book 2	JamesFKuroseandKeithWRoss ComputerNetworking:ATopDownApproach	Sixth	Pearson Education	2013
Reference 1	AndrewS.Tanenbaum,ComputerNetworks	Fourth	Prentice Hall	2003
Reference 2	Schwartz M, Telecommunication Networks, Protocols, Modeling and Analysis	Second	Addison-Wesley	1987
Reference 3	WilliamStallings,DataandComputerCommunications	Eighth	Prentice Hall	2007
Reference 4	RFC 1661 document on Point-to-Point Protocol (PPP)			July 1994

DIGITAL VLSI DESIGN (4-0-0-0-4)

Subject Code: UE19EC302 **No. of Hours: 56**

Faculty: RRC:Prof.SSR/Prof.AKY/Prof.HN/Prof.SML

ECC: Dr. TS/Prof.MA

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
UNIT 1: Introduction to MOS Inverters (Static Characteristics)				
1	R1: Chap 1(1.4,1.5), Chap 5 (5.1 – 5.4) & Chap 12 (12.4& 12.6)	VLSI design Methodologies and Design Flow (1.4 &1.5)	22%	22%
2		Introduction to inverters (5.1)		
3-5		Resistive-Load Inverter (5.2)		
6-8		Inverters with n-Type MOSFET Load(5.3)		
9-11		CMOS Inverter (5.4)		
12-13		Basic BiCMOS Circuits: Static Behavior, BiCMOS Applications (12.4 & 12.6)		
Unit 2: Fabrication of MOSFETs & Circuit Design Process				
14-15	R1:Chap 2 (2.1 – 2.5) R1:Chap 7 (7.4)	NMOS fabrication, CMOS fabrication, p-well, n-well, twin-tub process **(2.2 & 2.3)**	19%	41%
16 -17		MOS layers, Lambda based design rules, contact cuts **(2.4)**		
19 -22		Stick diagrams and Layout diagrams – nMOSdesignstyle(simplenMOSCircuits) **(3.2)**		
23 -24		Complex Logic Circuits **(7.4)**		
Unit 3: Basic circuits concepts and Scaling of MOS				
25	R2:Chap 4 (4.1-4.8.1) R2:Chap 5 (5.1 &5.2)	Sheet resistance **(4.1 & 4.2)**	14%	55%
26 -27		Area capacitance **(4.3, 4.4 & 4.5)**		
28 - 29		Delay unit, Inverter delays, Rise time and fall time estimation **(4.6 & 4.7)**		
30		Cascaded inverters as drivers **(4.8.1)**		
31 - 32		Scaling models, Scaling factors, parameters for scaling **(5.1 &5.2)**		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 4: Advanced Techniques in CMOS logic circuits and Adders				
33	R1: Chap 9(9.2 & 9.5) R3:Chap 9(9.1-9.5) and Chap 12(12.1-12.4)	CMOS Transmission Gates and Pass Transistors **(R1,9.2)**	25%	80%
34		Mirror circuits **(R3, 9.1)**		
35		Pseudo nMOS, Tristate circuits **(R3,9.2 & 9.3)**		
36		Clocked CMOS, circuits **(R3,9.4)**		
37 - 38		Domino logic, Dynamic CMOS logic **(R1,9.5)**		
39 - 40		Adders : Bit adder circuits **(12.1)**		
41-42		Carry Look - ahead Adder **(12.3)**		
43 - 44		Other High speed adders – Carry Skip, Carry Select & carry Save Adder **(12.4)**		
Unit 5: Sequential CircuitsDesign				
45 - 48	R1: Chap10 (10.2 & 10.3) R4: Chap 7 (7.2 &7.3)	Basic SRAM and DRAM cell **(10.2 & 10.3)**	20%	100%
49 - 51		Sequencing static circuits, Sequencing Methods, Max-Delay Constraints, Min-Delay Constraints **(7.2)**		
52 - 53		Time Borrowing, Clock Skew, Problems on Max and Min Delay Constraints at design level **(7.2)**		
54 - 56		Circuit design of latches and flip-flops - Conventional CMOS Latches and Flip- Flops, Resettable Latches and Flip- flops, Enabled Latches andFlip-Flops **(7.3, upto – 7.3.5)**		

Note:

Reference Books:
R1: CMOS Digital Integrated Circuits Analysis And Design, Sung-Mo (Steve) Kang,
R2: Basic VLSI Design, Douglas A. Pucknell& Kamran Eshraghian 3rd Edition.
R3: Introduction to VLSI circuits and systems, Uyemura, John P. (2002).
R4: CMOS VLSI design A Circuits and Systems Perspective,NeilWeste and David Harris, 3rd Edition.

CONTROL SYSTEMS (4-0-0-0-4)

Subject Code: UE19EC303 **No. of Hours: 56**

Faculty: RRC-Dr. MA/ Dr. ST/Prof.KS/Prof. RM/Prof.TE

ECC-Dr. SB/Prof. PD

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
UNIT 1: Mathematical Models of Systems				
1	**T1: 2.1 - 2.7**	Introduction	21.4 %	21.4%
2		Open and Closed Loop Control Systems		
3		Differential Equations of Physical Systems		
4		Differential Equations of Physical Systems		
5		Differential Equations of Physical Systems		
6		Linear Approximations of physical Systems		
7		The Laplace Transform		
8		The Transfer Function of Linear Systems		
9		Block Diagram Models		
10		Block Diagram Models		
11		Signal-Flow Graph Models		
12		Signal-Flow Graph Models		
UNIT 2: Feedback Control System Characteristics				
13	**T1: 4.1 - 4.6**	Introduction	17.9 %	39.3 %
14		Error Signal Analysis		
15		Sensitivity of Control Systems to Parameter Variations		
16		Sensitivity of Control Systems to Parameter Variations		
17		Control of the Transient Response of Control Systems		
18		Disturbance Signals in a Feedback Control System		
19		Steady State Error		
20		Steady State Error		
21		Steady State Error		
22		Steady State Error		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
UNIT 3: Performance of feedback Control systems				
23	**T1: 5.1 - 5.6 R1: 10.6, Page. No: 477 - 483**	Introduction	17.9 %	57.2 %
24		Test Input Signals		
25		Performance of a Second Order System		
26		Performance of a Second Order System		
27		Effects of a Third Pole and a Zero on the Second Order System Response		
28		The ***s*** – Plane Root Location		
29		the Transient Response		
30		The Steady – State Error of Non unity Feedback Systems		
31		Introduction to Controllers, PD Controller		
32		PI, PID Controllers		
UNIT 4:The stability of linear feedback systems				
33	**T1: 6.1 - 6.3 Root Locus method T1: 7.1 - 7.3 Frequency Response methods T1: 8.1, 8.2, 8.4**	The Concept of Stability	21.4%	78.6 %
34		The Routh – Hurwitz Stability Criterion		
35		The Routh – Hurwitz Stability Criterion		
36		The Relative Stability of Feedback Control Systems		
37		Introduction Root locus Concept		
38		The Root Locus procedure		
39		The Root Locus		
40		The Root Locus		
41		Introduction, Frequency Response Plots		
42		Bode Diagram		
43		Bode Diagram		
44		Performance Specifications in the Frequency Domain		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
UNIT 5: Stability in the Frequency Domain				
45	**T1 : 9.1 - 9.4** **Design of Feedback Control Systems** **T1: 10.1 - 10.4, 10.6, 10.8**	Introduction, Mapping Contours in the s – Plane	21.4 %	100%
46		The Nyquist Criterion		
47		The Nyquist Criterion		
48		Relative Stability and the Nyquist Criterion		
49		Introduction, Approaches to System Design		
50		Cascade Compensation Networks		
51		Phase – Lead Design Using the Bode Diagram		
52		Phase – Lead Design Using the Bode Diagram		
53		Phase – Lead Design Using the Bode Diagram		
54		System Design Using Integration Networks		
55		Phase-Lag Design Using Bode Diagram		
56		Phase-Lag Design Using Bode Diagram		

Assignments: Assignments on PBL to be given at regular intervals aimed at hands on experience through tools like Matlab, Simulink.

Text Book	"Modern Control systems", R.C. Dorf and R.H. Bishop, 11th Edition, PEARSON Education 2009.
Recommended Books	
1.	Control Systems Engineering, I.J.Nagrath and M.Gopal, 5th edition, New Age International Publications, 2007.
2.	"Modern Control Engineering", K. Ogata, 5th edition, Pearson Education Asia, 2010.
3.	"Control Systems Engineering," N. Nise, Wiley India, 2018.

Computer Communication Networks Laboratory (1-0-0-2)

Subject Code: UE19EC304

Faculty : Prof. MR **No. of Weeks/Hrs: 14 / 28 hrs**

Software used: Wireshark, GNS3, Python

Exp #	Week #	Experiment	% of Portion Covered	
			Reference	Cumulative
		Cycle -1		
1	Week-1	Introduction to Wireshark, GNS3 and Python	7.15	57.2
2	Week-2	Analyse GET and Conditional GET under HTTP using Wireshark	7.15	
3	Week-3	Analyse the downloading of embedded objects in a web-page using Wireshark	7.15	
4	Week-4	Analyse the DNS query and response using Wireshark	7.15	
5	Week-5	Analyse the TCP fragmentation when downloading large files from a web-server using Wireshark	7.15	
6	Week-6	Animations:Studentresources **https://wps.pearsoned.com/ecs_kurose_compnetw_6/216/55463/14198700.cw/index.html**	7.15	
7	Week-7	Analyse TCP connections to a web-server using Wireshark	7.15	
8	Week-8	Write and Analyse socket programs using Python	7.15	
		Cycle -2		
9	Week-9	Design a simple LAN to demonstrate static addressing and static routing using GNS3	7.15	42.8
10	Week-10	Design a network with 4 subnets to demonstrate static addressing and dynamic routing using GNS3	7.15	
11	Week-11	Design a 1-hop network to demonstrate dynamic addressing and dynamic routing using GNS3	7.15	
12	Week-12	Design a 2-hop network to demonstrate dynamic addressing and dynamic routing using GNS3	7.15	
13	Week-13	Design a 2-hop network to demonstrate static and dynamic NAT configurations	7.15	
14	Week-14	Open-ended experiment- Team wise Demo by students	7.15	
Total				**100%**

Information:

- 14 weeks/ Weekly 2 hours
- 13 Experiments (including Introduction) + Open-ended experiment (in a team of 3 students)
- Students to maintain Record work & Observation Note Book
- Lab Manual can be used as reference
- Open-ended experiment at end of course

Assessment:

1. ISA based on Observation book, record work and end-semester-quiz/viva. 50%
2. FSA – Conduction of experiment + Viva - 50%

Reference: **Lab Manual – Aug-Dec 2021**

DIGITAL VLSI DESIGN LABORATORY (0-0-2-0-0)

Subject Code: UE19EC305

Faculty:Prof.SSR/Prof.AKY/Prof.HN/Prof.SML

List of experiments

Sl #	Experiment name
1.	Introduction to EDA Tool with Layout Design Rules
2.	Design and determine Critical voltages, Noise Margin NM_H and NM_L of Resistive loaded Inverter
3.	Design Saturated NMOS load Inverter and determine 1. Critical voltages, Noise Margin NM_H andNM_L. 2. Draw the Layout and do the following Verifications a. Design Rule Check(DRC) b. Layout Vs Schematic Match(LVS) c. Generate the Parasitic View of theLayout
4.	Design symmetrical CMOS inverter and determine 1. Critical voltages, Noise Margin NM_H and NM_L, PowerDissipation 2. Draw the Layout and do thefollowing Verifications a. Design Rule Check(DRC) b. Layout Vs Schematic Match(LVS) c. Generate the Parasitic View of theLayout
5.	Design NAND gate in CMOS technology. 1. PowerDissipation 2. Determine rise time, fall time,propagation delay 3. Determine dynamic powerdissipation 4. Draw the Layout and do thefollowing Verifications a. Design Rule Check(DRC) b. Layout Vs Schematic Match(LVS) c. Generate the Parasitic View of theLayout
6	Design NOR gate in CMOS technology. 1. PowerDissipation 2. Draw the Layout and do thefollowing Verifications a. Design Rule Check(DRC) b. Layout Vs Schematic Match(LVS) c. Generate the Parasitic View of theLayout
7	Realization of the following circuits using Transmissiongates i) 4:1MUX ii) 1 bit FullAdder
8	Determine propagation delay and dynamic power dissipation of CMOS SR latch based on two input NOR gates
9	Determine propagation delay and dynamic power dissipation of CMOS Master Slave JK flip-flop based on two input NOR gates
10	Determine propagation delay and dynamic power dissipation of edge triggered MS D FF.
11	Design Asynchronous and Synchronous Counter using Edge triggered DFF instance.

INFORMATION THEORYAND CODING (4-0-0-4-4)

Subject Code: UE19EC311 **No. of Hours: 56**

Faculty: Dr. AT

Pre-Requisite Course: knowledge of Digital Communication

Class #	Chapter Title/Reference Literature	Topics to be Covered	% Portions Covered	
			Reference chapter	Cumulative
1-2	UNIT-I Information Theory T1: Ch 1	Uncertainty, Information and Entropy	20	20
3-4		Joint Entropy		
5-8		Conditional Entropy and Mutual Information		
9-12		Coding Theorem, Shannon-Fano Coding, Huffman coding.		
13-16	UNIT-II Channel Capacity T1: Ch 2	Discrete Memoryless channels	20	40
17-18		Channel Capacity, Channel Coding Theorem		
19-23		Differential entropy and Mutual Information for Continuous Ensembles		
24		Spectral Efficiency		
25-27	UNIT-III Linear Block Code T1: Ch 3	Introduction to algebra, methods of controlling errors, types of codes, types of errors	20	60
28-30		Linear Block Codes: Matrix description, Syndrome, minimum distance, error detection and error correction		
31		Decoding using the Standard arrays		
30-35		Cyclic codes: Encoding using an (n-k) bit shift register. Syndrome calculation, error detection and correction		
36-37	UNIT-IV Convolutional Codes T1: Ch 7	Time domain approach, transform domain approach,	20	80
38-40		Tree and Trellis diagrams,		
41-42		The Viterbi Algorithm		
43-46		Turbo codes		
47-50	UNIT-V Advanced Coding Techniques T2: Ch 16, Ch 17	LDPC codes: General Description, Characteristics, Encoding and Decoding.	20	100
51-52		Rateless codes		
53		Raptor codes, coding for data storage.		
54-56		Polar codes.		

References:

Book Type	Code	Title & Author	Publication info	
			Publisher	Edition
Text Book 1	T1	Information Theory, Coding and Cryptography by Ranjan Bose	Tata McGraw-Hill Education	2nd edition, 2008
Text Book 2	T2	Error Control Coding: Fundamentals and Applications by Daniel J. Costello and Shu Lin	Pearson	2nd edition, 2011

ADVANCED DIGITAL DESIGN(4-0-0-4-4)

Subject Code: UE19EC313 **No. of Hours: 56**

Faculty: Dr. KSK

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 1 - RTL Coding using Verilog HDL				
1	(Textbook-1) Chap. 3,4,5,6	Review of Verilog HDL	15%	15%
2		RT Level Combinational Circuit		
3		Regular Sequential Circuit		
4		FSM Design and RTL Coding for FSM		
5		Verilog RTL Coding styles for FSM		
6		FSM -Moore and Mealy		
7		Circular FIFO, FSMD Example		
8		FSMD Example & Code Coverage		
9		Cadence NCSim Demo		
10		Code Coverage Demo		
11		Review of Verilog HDL		
Unit 2 - Timing Conventions				
12	(Reference -1) Chapter-9	Skew and Jitter Analysis	33%	48%
13		Allowable Clock rates and timing design		
14		Timing Nomenclature		
15		Timing Properties: Delay elements		
16		Timing Properties: Combinational logic		
17		Timing Properties: Clocked Storage element		
18		Eye Diagram and analysis		
19		Encoding aperiodic events and encoding periodic signals		
20		On-Chip Clock distribution		
21		Demo of timing properties- Verilog simulation		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 3 – Synchronization				
22	(Reference -1) Chapter-10	Importance of Synchronization strategies	23%	71%
23		Synchronization fundamentals		
24		Synchronization failure and metastability		
25		Classification of Signal Clock Synchronization		
26		Synthesis Demo		
27		Synthesis Demo		
28		Static timing analysis (STA)		
29		Static timing analysis (STA)& Demo		
30		STA Demo		
Unit 4- Synchronizer Design				
31	(Reference -1 & 2) Chapter-10	Mesochronous Synchronizers	17%	88%
32		Mesochronous Synchronizers		
33		Plesiochronous synchronizers		
34		Plesiochronous synchronizers		
35		Plesiochronous synchronizers		
36		Asynchronous Synchronizers		
37		Asynchronous Synchronizers		
38		Asynchronous Synchronizers		
39		Stoppable Clocks and protocols		
40		Solutions to Clock Domain Crossing		
41		Dual Clock FIFO Solution		
42		CDC demo -1		
43		CDC demo -2		
44		CDC demo -3		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 5–Resets and Pipelining				
45	(Reference 2) Chap. 2,3,4,6	Theory of Metastability	12%	100%
46		MTBF and avoiding metastability		
47		Metastability Test Circuit and simulation		
48		Reset Design Strategy		
49		Reset Synchronizer and glitch filtering		
50		Asynchronous Reset Removal		
51		Pipelining		
52		Performance improvement from pipelining		
53		Example of DLX processor and pipelining principles		
54		Demo of Metastability Test circuitry simulation		
55		Demonstration of pipelining		
56		Demonstration of Pipelining		

Text Books:

1. Pong P Chu, “FPGA Prototyping by Verilog Examples: Xilinx Sparta-3 Version”, WileyBlackwell, ISBN-13: 978-0470185322, 2008.

References:

1. William J Dally, John W Poulton, “Digital Systems Engineering”, Cambridge University Press, ISBN-10: 052106175X -1998.
2. Mohit Arora, “The Art of Hardwre Architecture: Design Methods and Techniques for DigitalCircuits”, Springer-2012, ISBN-13: 978-1461403968.
3. Clifford E Cummings, Arturo Salz, “System Verilog Event Regions, Race Avoidance and Guidelines”, Sunburst DesignIncWhitepaper.

http://www.sunburst-design.com/papers/CummingsSNUG2006Boston_SystemVerilog_Events.pdf.

4. Clifford E Cummings, “: Clock Domain Crossing (CDC) Design & Verification Techniques”, http://www.sunburstdesign.com/papers/CummingsSNUG2008Boston_CDC.

ELECTRONIC DESIGN AUTOMATION- VERILOG TO ROUTING (4-0-0-0-4)

Subject Code: UE19EC316 **No. of Hours: 56**

Faculty: EC Campus: Dr. MP

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
UNIT-1 Introduction to EDA:				
1-12	(R1:Ch1, R4: Ch1,2,3,4)	Introduction, History of Design Automation, Target Technologies: PLA, PLD, Standard Cells, FPGAs, ASICs, Structured ASICs, Processors and SOCs, MPSoCs, Performance Metrics: Time, Area, Power	**25%**	**25%**
UNIT-II High-level Synthesis:				
12-24	(R2:Ch1 & Ch 2)	Scheduling, Allocation, Timing measurements, Sources of Parallelism, HLS pragmas, Case Study in HLS, Performance comparison: RTL Versus HLS	**25%**	**50%**
UNIT-III Logic Synthesis and Technology Mapping:				
25-36	(R1: Ch 7,8,9)	Introduction to Logic Synthesis, Binary Decision Diagrams, Combinatorial Logic Optimisations, Two-level and Multi-level Logic Optimisation, Sequential circuit optimisation: retiming, restructuring, resynthesis, And-Inverter Graphs, Boolean Matching, Logic decomposition. Gate sizing, logic restructuring, covering algorithms and structural matching. Lab exercise on elaboration and logic optimisation.	25%	75%
UNIT-IV Placement and Floor planning				
36-46	(R3: Ch 4, Ch 7)	Hard problems and NP-completeness, Simulated Annealing Genetic Algorithms. Lab exercises on placement algorithms.	12%	87%
UNIT-V Routing				
46-56	(R4: Ch 5,R3:Ch9)	Introduction to routing, Area routing, Channel routing, Global routing, Maze routing algorithm. Lab exercise on routing and timing analysis using VPR	13%	100%

References:

Book Type	Code	Title & Author	Publication Info		
			Edition	Publisher	Year
TextBook	R1	Synthesis and Optimization of Digital Circuits, Giovanni De Micheli	1st	Tata McGraw-Hill Education	2004
Reference Book - 1	R2	Parallel Programming for FPGAs, Ryan Kastner and Janarbek Matai and Stephen Neuendorffer	1st	https://arxiv.org/pdf/1805.03648.pdf	2018
Reference Book - 2	R3	Algorithms for VLSI Design Automation, Sabih H. Gerez	2nd	Wiley Publishing	1998
Reference Book - 3	R4	FPGA Architecture: Survey and Challenges, Ian Kuon, Russell Tessier and Jonathan Rose	1st	https://arxiv.org/pdf/1805.03648.pdf	2004

DIGITAL IMAGE PROCESSING (4-0-0-0-4)

Subject Code: UE19EC317 **No. of Hours: 56**

Faculty: RR Campus: Dr. ST

EC Campus: Dr. SSK

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
UNIT-1 Digital Image Fundamentals:				
1	T1 1.1, 1.4, 1.5, 2.1, 2.3, 2.4, 2.5 and 2.6	Introduction and overview of course	19.64	19.64
2		WhatisdigitalImageProcessing, types of images		
3-4		FundamentalStepsinDigitalImageProcessing , ComponentsofanImageProcessingSystem		
5-6		Visual Perception, Sensing and acquisition, Image formation model		
7-8		ImageSamplingandQuantization		
9-11		Some basic relationship between pixels LinearandNonlinearoperations		
UNIT-2 ImageTransforms				
12-13	R1 5.2, 5.4 - 5.11 & 5.13	2-DorthogonalandUnitarytransforms	21.43	41.07
14-15		1-Dand2-dDFT		
16-17		Cosine,Sine, Hadamard transforms		
18-19		Haar , Slant transforms		
20-21		Karhunen-loeve transforms		
22-23		SingularvalueDecomposition		
UNIT-3 Image Enhancement:				
23-25	T1:3.1 - 3.7 R1:7.1-7.6	Basic Gray Level transformations, histogram processing, Enhancement using ALU operations	21.43	62.5
25-26		Basics of spatial filtering, spatial operations		
27-28		Smoothing spatial filters sharpening spatial filters		
29-30		Image Enhancement in Frequency domain: Ideal low pass filters		
31-32		Butterworth low pass filters, Gaussian low pass filters		
33-34		Sharpening filters, Unsharp masking, High boost filtering, Notch filters, Homomorphic filtering.		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
UNIT-4 Image filtering and Restoration:				
35-36	T1: 5.1 - 5.4, 5.7- 5.9 R1: 8.2, 8.3, 8.6, 8.7, 8.8	Image observation models, Noise Models	19.64	82.14
37-39		Restoration in the presence of noise only-Spatial Filtering		
40-42		Periodic noise reduction by frequency domain filtering		
43-45		Inverse and Wiener filtering, least square filters		
UNIT-5				
46-48	**Colorimageprocessing:** T1: 6.1 – 6.6, 6.8	ColorFundamentals,ColorModels,Pseudocolor Image Processing	17.86	100
49-51		BasicsofFull-ColorImage Processing, ColorTransformations		
52-53		SmoothingandSharpening		
54-55		NoiseinColorImages		

Reference Books:

Book Type	Code	Title & Author	Publication Info		
			Edition	Publisher	Year
Text Book	T1	"Digital Image Processing", R.Gonzalaz and Woods	4th	Prentice Hall	2018
Reference Book - 1	R1	Fundamentals of Digital Image Processing, Anil K Jain	1st	Pearson Education Pvt. Ltd.	2004
Reference Book - 2	R2	S Jayaraman, S Esakkirajan and T Veerakumar, "Digital Image Processing"	1st	Mc Graw Hill	2009

PATTERN CLASSIFICATION (4-0-0-0-4)

Subject Code: UE19EC318 **No. of Hours: 56**

Faculty : Dr. JMK

Class #	Chapter Title / Reference Literature	Topics to be Covered	% of portions covered	
			Reference	Cumulative
UNIT I : Introduction and Bayesian Decision Theory				
1	**Richard o Duda- 1.1, 1.2, 1.3, 1.4, 1.5, 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.9, 2.10**	Machine perception and its example	19.6	19.6
2		pattern recognition systems, the design cycle; learning and adaptation		
3		Bayesian decision theory Introduction		
4		Bayesian decision theory - continuous features		
5		minimum-error-rate classification		
6		Classifiers		
7		discriminant functions		
8		normal density		
9		discriminant functions for the normal density		
10		Bayesian decision theory - Discrete features		
11		Missing and noisy features.		
UNIT II : Maximum-likelihood and Bayesian Parameters Estimation				
12	**Richard o Duda- 3.1, 3.2, 3.3, 3.4, 3.5, 3.7, 3.8, 3.10**	Maximum-likelihood estimation	19.6	39.2
13		Maximum-likelihood estimation		
14		Bayesian estimation		
15		Bayesian parameter estimation		
16		Bayesian parameter estimation :Gaussian case		
17		Bayesian parameter estimation :General theory		
18		problems of dimensionality		
19		component analysis		
20		Discriminants		
21		Hidden Markov models.		
22		Hidden Markov models.		
UNIT III :Non-parametric Techniques				
23	**Richard o Duda- 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.9**	Density estimation	19.6	58.8
24		Parzen windows		
25		Parzen windows		
26		k_n-nearest-neighbor estimation		
27		Nearest-neighbor rule		
28		Metrics		
29		Metrics		
30		Nearest - Neighbor classification		
31		Nearest - Neighbor classification		
32		Approximation by series expansions		
33		Approximation by series expansions		

Class #	Chapter Title / Reference Literature	Topics to be Covered	% of portions covered	
			Reference	Cumulative
UNIT IV : Linear Discriminant Functions				
34	**Richard o Duda- 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11, 5.12**	Linear discriminant functions and decision surfaces	19.7	78.5
35		generalized linear discriminant functions		
36		two-category linearly separable case		
37		minimizing the perceptron criterion function;		
38		relaxation procedures and nonseparablebehaviour		
39		minimum squared-error procedures		
40		Ho-Kashyap procedures		
41		linear programming algorithms		
42		support vector machines		
43		support vector machines		
44		Multicategory generalizations		
UNIT V: Unsupervised Learning				
45	**Richard o Duda- 10.1, 10.2, 10.3, 10.4, 10.5, 10.6, 10.7, 10.10, 10.11, 10.13, 10.14**	Mixture densities and Identifiability	21.5	100
46		Maximum-likelihood estimates		
47		Application to normal mixtures		
48		Application to normal mixtures		
49		unsupervised Bayesian learning		
50		unsupervised Bayesian learning		
51		Data description and clustering		
52		criterion functions for clustering and hierarchical clustering		
53		problem of validity		
54		on-line clustering		
55		component analysis		
56		Low-dimensional representation and multidimensional scaling.		

Text Book:

1. "Pattern Classification"Richard O. Duda, Peter E. Hart and David G. Stork, 2nd edition, John Wiley, 2001.

Reference Books:

1. "Pattern Recognition and Image Analysis,"EartGose, Richard Johnsonburg and Steve Joust, Prentice-Hall of India, 2003.
2. "Pattern Recognition and Machine Learning,"Christopher M. Bishop, 3rd edition, Springer, 2007.
3. "Statistical Pattern Recognition," Andrew R. Webb, 2nd edition, John Wiley, 2002.

WIRELESS COMMUNICATION (4-0-0-0-4)

Subject Code: UE19EC321 **No. of Hours: 56**

Faculty: Prof.BVK

ECC: RRK

Class	Chapter Title/ Reference Literature	Topic to be covered	% of Portion covered	
			Reference Chapter	Cumulative
UNIT-1Overview of Wirelesscommunication,Path Loss & Shadowing, Mobile Radio Propagation,Path Loss & Shadowing				
1	**T1: Chapter 1** Sec: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6 Page 1-24 **T1: Chapter 2** Sec: 2.1, 2.2, 2.3, 2.4, 2.4.2, 2.4.2, 2.4.4 Page 27-41 **R1: Chapter 3** Sec: 3.10.3, 3.10.4 Page 116-120 **T1: Chapter 2** Sec: 2.5.3, 2.5.4, 2.5.5, 2.6, 2.9, 2.10 Page 44-48 & 53-56	History andvision of Wirelesscommunication,	22	22
2		Technical issues, Currentwireless systems		
3		Thewirelessspectrum,StandardsofWirelesscommunication		
4		Radio Wavepropagation; Transmit &receive signal model		
5		Freespace path loss		
6		Raytracing : Two Ray Model		
7		Ten Ray Model, General Ray Tracing, Local Mean Received Power		
8		Empirical path lossmodel		
9		Simplified path loss model		
10		Outrage probabilityunderpathlossshadowing		
11		Cellcoveragearea		
12		Numerical		
UNIT-2Statistical Multipath Channel Models, Mobile Radio Propagation, Statistical Multipath Channel Models, Mobile Radio Propagation				
13	**T1: Chapter 3** Sec: 3.1, 3.2.1, 3.2.2 Page 64-78 **R1: Chapter 4** Sec: 4.7.3 Page: 186-188 **T1: Chapter 3** Sec: 3.3 Page 82-84 **R1: Chapter 4** Sec: 4.4 Page: 159-160 **R1: Chapter 4** Sec: 4.4.1-4.4.2, 4.4.3, 4.5, 4.5.1, 4.5.2, 4.6, 4.6.1, 4.6.2 Page: 160-176	Time varying channelimpulseresponse	22	44
14		Narrowband fading model, Autocorrelation, Cross-correlation		
15		Power spectral density, Envelope and power distributions		
16		Level crossing rate and average fade duration		
17		Wideband fading models, Parameters of mobile multipath channels		
18		Power delay profile: Time dispersion parameters, Coherence bandwidth		
19		Doppler spread and coherence time		
20		Types of small-scale fading		
21		Rayleigh fading distribution		
22		Rayleigh fading distribution		
23		Numerical		
24		Numerical		

Class	Chapter Title/ Reference Literature	Topic to be covered	% of Portion covered	
			Reference Chapter	Cumulative
UNIT-3 Spread Spectrum, Multiuser Systems				
25	**T1: Chapter 13** Sec: 13.1, 13.2, 13.2.1, 13.2.2, 13.2.3, 13.2.4, 13.3, 13.4, 13.4.1 Page 403-428 **T1: Chapter 14** Sec: 14.1, 14.2, 14.2.1, 14.2.2, 14.2.3, 14.2.4, 14.2.5 Page 452-460	Spread spectrum principles	22	66
26		Direct sequence spread spectrum (DSSS)		
27		Spreading codes for ISI rejection: Random, Pseudorandom and m Sequences		
28		Generation of spreading codes		
29		Synchronization for DSSS, Rake receivers		
30		Numerical		
31		Frequency Hopping Spread Spectrum (FHSS)		
32		MultiuserDSSSsystems, Spreading codes for multiuser DSSS: Gold codes		
33		Numerical		
34		Kasami codes and Walsh Hadamard codes		
35		Uplinkand downlink channels, FDMA, TDMA		
36		CDMA,SDMA,Hybridtechniques, MultiuserFHSSsystems		
UNIT-4 Cellular Systems and Infrastructure-Based Wireless Networks,Capacity of Wireless Channels,Diversity				
37	**T1: Chapter 15** Sec: 15.1, 15.2, 15.3, 15.3.1, 15.3.2, 15.4, 15.5, 15.6, 15.6.1, 15.6.2 Page 505-528 **T1: Chapter 4** Sec: 4.1, 4.2, 4.2.1, 4.2.2, 4.2.3, 4.2.4 Page 99-111 **T1: Chapter 7** Sec: 7.1 , 7.2, 7.3 Page: 204-220	Cellularsystemfundamentals	17	83
38		Channel Reuse		
39		SIR and User capacity: Orthogonal systems (TDMA/FDMA)		
40		Nonorthogonal systems (CDMA)		
41		Interference reduction techniques, Dynamic resource allocation		
42		Fundamentalratelimits		
43		Capacity of wirelesschannels:CapacityofAWGN		
44		Capacity of Flat fadingmodels		
45		Capacity with outage, CSI at transmitter and receiver, CapacityVsReceiverdiversity		
46		Diversity:Realization of independentfading paths, Receiverdiversity,Transmitter diversity		
UNIT-5 Multicarrier Modulation				
47	**T1: Chapter 12** Sec: 12.1, 12.2, 12.4, 12.4.2, 12.4.3, 12.4.4, 12.4.5 Page: 374- 380, 383-392	Data transmission usingmultiplecarriers	17	100
48		Multicarriermodulation with overlapping sub channels		
49		Discreteimplementationofmulticarrier modulation, TheDFT and its properties		
50		Thecyclic prefix		
51		Numerical		
52		Orthogonalfrequency-divisionMultiplexing		
53		MatrixrepresentationofOFDM		
54		Vectorcoding		
55		Numerical		
56		Numerical		

Text Book:

1) "Wireless Communications", Andrea Goldsmith, Cambridge University Press, 2011.

Reference Books:

1) "Wireless Communications: Principles and Practices", T. S. Rappaport, 2nd Edition, Prentice Hall, 2002.
2) "Fundamentals of Wireless Communications", David Tse and Pramod Vishwanath, Cambridge University Press, 2009.

OPERATIONS RESEARCH (4-0-0-4-4)

Subject Code: UE19IE301 **No. of Hours: 56**

Faculty: Prof.NLJ

Class	Chapter Title/ Reference Literature	Topic to be covered	% of Portion covered	
			Reference Chapter	Cumulative
Unit 1-Introduction				
1-10	Txt 1: 1.1, 1.2, 1.4, 1.8, 1.9, 1.11, 1.12, 3.1 to 3.10	Introduction-complete overview of the course with the course contents.	**18**	**18**
		Definition, scope of operations research approach and limitations of OR.		
		Brief history, characteristics of OR, OR model-definition and .		
		Classification of OR models, solving the OR models, Phases of OR, Mathematical formulation of LP problems.		
		Problems on Formulation		
		Problems on Formulation		
		Graphical solution method-procedure		
		Solving Problems by using Graphical solution method		
		Solving Problems by using Graphical solution method		
		Special cases in Graphical method-Unbounded solution, Alternate optimum solution and Infeasible solution with problems on each case		
Unit 2 Linear programming				
11-22	Txt 1: 5.1, 5.3, 5.4, 5.7, 5.8, 5.11 5.5-4, 7.3, 7.4, 7.7-1, 8.1 to 8.5	Canonical and Standard form of LPP, converting inequalities into equations using slack, surplus and unrestricted variables, Defining Basic feasible solution.		
		Finding the solution to the given LPP by enumerating all basic solutions		
		Simplex method-procedure and problems		
		Simplex method-procedure and problems		
		Artificial starting solution by using Artificial variables: Big-M Simplex method - procedure and problems.		
		Artificial starting solution by using Artificial variables: Big-M Simplex method - procedure and problems.		
		Two-phase Simplex method-procedure and problems		
		Two-phase Simplex method-procedure and problems		
		Special cases in Simplex method-problems		
		Special cases in Simplex method-problems		
		Concept of Duality-Formulation and problems		
		Dual Simplex method-procedure and problems		

Class	Chapter Title/ Reference Literature	Topic to be covered	% of Portion covered	
			Reference Chapter	Cumulative
Unit 3 Transportation and Assignment problems				
23-34	Txt 1: 11.1, 11.4, 11.8, 11.9, 11.9-1, 11.9-7, 11.10, 11.12, 12.1, 12.4 to 12.7	Formulation of Transportation model, Definition of Basic feasible solution	**21**	**60**
		Basic feasible solution by using different methods: North-west corner method-procedure and problems		
		Basic feasible solution by using Row-minima method-procedure and problems, Basic feasible solution by using Column-minima method-procedure and problems, Basic feasible solution by using Matrix-minima method-procedure and problems.		
		Basic feasible solution by using Vogel's Approximation method-procedure and problems		
		Optimality by MODI method-procedure and problems		
		Optimality by MODI method-procedure and problems		
		Degeneracy in Transportation problem		
		Unbalanced Transportation problem, Maximization problem		
		Assignment model-Formulation, differences between Transportation problem and Assignment problem, Hungarian method-procedure and problems, Unbalanced Assignment problems.		
		Assignment model-Formulation, differences between Transportation problem and Assignment problem, Hungarian method-procedure and problems, Unbalanced Assignment problems.		
		Travelling-salesman problem: Formulation and problems		
		Travelling-salesman problem: Formulation and problems		

Class	Chapter Title/ Reference Literature	Topic to be covered	% of Portion covered	
			Reference Chapter	Cumulative
Unit 4 PERT-CPM Techniques				
35-46	Txt 1: 25.1, 25.5, 25.6, 25.8, 25.9, 25.10	Steps in PERT/CPM techniques, Network construction, basic definitions, rules for drawing network diagram.	**21**	**81**
		Examples on constructing a network diagram		
		Examples on constructing a network diagram		
		Numbering the events-Labelling rule, Time estimates and Critical path in network analysis.		
		Forward-pass computations, Backward-pass computations- examples		
		Forward-pass computations, Backward-pass computations- examples		
		Forward-pass computations, Backward-pass computations- examples		
		Determination of Critical paths using PERT and CPM techniques- problems		
		Determination of Critical paths using PERT and CPM techniques- problems		
		Determination of Critical paths using PERT and CPM techniques- problems		
		Cost analysis and crashing of networks		
		Cost analysis and crashing of networks, Sensitivity analysis		
Unit 5 Game theory and Queuing theory				
47-56	Ref 1: 17.1, 17.2, 17.6.1 to 17.6.3	Game theory: Definition, characteristics, two-person zero sum game, payoff matrix.	**18**	**100**
		Games with Saddle point, Games without saddle points: Algebraic method-procedure and problems		
		Games without saddle points: Algebraic method-procedure and problems		
		Games without saddle points: Arithmetic method-procedure and problems, principle of dominance		
		Games without saddle points: Arithmetic method-procedure and problems, principle of dominance		
		Games without saddle points: Arithmetic method-procedure and problems, principle of dominance		
		Graphical method for 2xn games-procedure and problems		
		Graphical method for mx2 games-procedure and problems Queuing theory: M/M/I Queuing system-problems		

		M/M/C Queuing system-problems		

Literature

Book Type	Code	Title & Author	Publication Info		
			Edition	Publisher	Year
Text Book	Txt 1	"Operations Research", S.D. Sharma	15th revised	Kedarnath Ramnath	2009-10
Reference Book	Ref 1	"Operations Research –An introduction", Hamdy A Taha	10th	Prentice Hall of India, private Ltd	2019

Real Time Operating Systems (4-0-0-0-4)

Subject Code: UE19EC323 **No. of Hours: 56**

Faculty: Prof.Bivas Bhattacharya.
Prof.Pavitra Y J

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
Unit 1				
1-10	R2 - Section 1.1	Introduction – Course overview	2	2
	R1 - Section 2.1	Goals of an OS	2	4
	R2 - Section 1.5 to 1.9	Operation of an OS	2	6
	R1 - Section 2.3	Principles of OS	2	8
	R1 - Section 2.6,2.7,2.10,2.11	Key features of classes of OS	2	10
	R1 - Section 2.4 and R2 - section 2.1	System performance and user services	2	12
	R2 - Section 2.7	Structure of an OS	2	14
	R2 - Section 2.7	Layered design of OS	2	16
	R2 - Section 1.7.3	Kernel and microkernel based OS	2	18
		Revision		18
Unit 2				
11-22	R2 - Section 3.1	Process concepts	2	20
	R1 - Section 3.2	PCB, 5 state model	2	22
	R1 - Section 3.2 and R2 - Section 3.2	Process scheduling	2	24
	R2 - Section 3.3	Operations on Processes, Threads	2	26
	R2 - Section 3.4	Inter Process Communication, Shared memory	2	28
	R2 - Section 3.4	IPC- Message Passing	2	30
	R2 - Section 3.6.3	Pipes, FIFO	2	32
	R2 - Section 6.5	Process synchronization, Semaphore	2	33
	R1 - Section 10.2	Priority inversion	2	34
	R1 - Section 10.2	Priority inheritance	2	38
	R1 - Section 10.2	Priority ceiling, mutex	2	40

		Revision	2	40

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
Unit 3				
23-34	R2 - Section 5.1	Scheduling Basic Concepts, preemptive and Non preemptive scheduling	2	42
	R2 – Section 5.2, 5.3.4	Round Robin Scheduling(RR)	2	44
	R2 - Section 5.3.2	Shortest Job First Scheduling(SJF)	2	46
	R2 - Section 5.3.1, 5.3.3	First Come First Serve(FCFS), Priority Scheduling	2	48
	R2 - Section 5.3.5, 5.3.6	Multilevel Queue Scheduling	2	50
	R2 - Section 19.5	Rate Monotonic Least Upper Bound	2	52
	R4 - Section 3.2, 3.3	Necessary and Sufficient Feasibility	2	56
	R4 - Section 3.6, 3.7	Deadline-Monotonic Policy, Dynamic-Priority Policies	2	58
	R4 - Section 4.2, 4.3	Worst-case Execution time, Intermediate I/O	2	60
	R4 - Section 4.4, 4.5	Execution Efficiency, IO Architecture	2	62
	R2 - Section 5.5	Multi processor scheduling	2	64
		Example Problems		64
Unit 4				
35-46	R2 - Section 8.1, 8.2	Memory management requirements	2	66
	R1 - Section 7.1	Memory management requirements	2	68
	R1 - Section 7.2	Memory Partitioning	2	70
	R1 - Section 7.2	Memory Partitioning	2	72
	R1 - Section 7.3	Paging	2	74
	R1 - Section 7.4	Segmentation	2	76
	R1 - Section 8.1	Hardware and Control Structures-Locality and Virtual Memory	2	78
	R1 - Section 8.1	Hardware and Control Structures- Paging,Segmentation	2	80
	R1 - Section 8.1	Hardware and Control Structures- Combined Paging and Segmentation, Protection and Sharing	2	82
		Example Problems	2	84

		Example Problems		84
		Revision		84

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
Unit 5				
47-56	T1 - Section 4.3	Defining an RTOS, implementing Real time Operating systems	2	86
	T1 - Section 4.7	Key Characteristics of an RTOS	2	88
	T1 - Section 14.2	An Outside-In Approach to Decomposing Applications	2	90
	T1 - Section 14.3	Guidelines and recommendations for identifying concurrency	2	92
		Lab1- Pipe,FIFO	2	94
		Lab2- Semaphore	2	96
		Lab3- Message Queue	2	98
		Lab4- Thread application	2	100
		Lab5- Thread application		100
		Revision		100

Text Book:

1. “Real-Time Concepts for Embedded Systems”, Qing Li and Carolyn, 1st Edition, CRC Press, 2003.

Reference Books:

1. Operating Systems, William Stallings, Pearson Publications,2018
2. “Operating System Concepts”, Silberschatz ,Galvin, Gagne, John Wiley & Sons
3. “Computer Architecture and Organisation”, J.P. Hayes, Second edition, Tata McGraw-Hill, 1988.
4. “Real-Time Embedded Systems and Components”, Sam Siewert, Cengage Learning India Edition, 2007

Artificial Neural Networks (4-0-0-0-4)

Subject code: UE19EC327

Faculty: Ms Swetha R. **Hours: 56**

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Individual	Cumulative
UNIT-1 Introduction:				
2Hrs	Text1: Chapters 1,2, 3 T1.1 to T1.7 T2.1 to T2.9 T3.1 to T3.7	What is a neural network? Human brain; models of a neuron; neural networks as directed graphs; feedback; network architectures;	25	25
3Hrs		**Learning Rules:** learning with and without a teacher. Error-correction learning; memory-based learning; Hebbian learning; competitive learning; Boltzmann learning; credit-assignment problem;		
4Hrs		Linear Neuron: Adaptive filtering problem; unconstrained optimization technique		
4Hrs		linear least-squares filters; least-mean-square algorithm; learning curves;		
UNIT-2 Perceptron				
5Hrs	Text1: Chapters 3, 4 T3.8 to T3.9 T4.1 to T4.16	**Single Layer:** Perceptron; perceptron convergence theorem.**Multilayer:** Preliminaries; back-propagation algorithm; XOR problem	25	50
2Hrs		BPA: heuristics for making the BPA perform better; output representation and decision rule		
3Hrs		Feature detection; back-propagation and differentiation; Hessian matrix; generalization; approximation of functions		
3Hrs		Cross-validation; network pruning techniques; virtues and limitation of back-propagation learning; accelerated convergence of back-propagation learning; supervised learning as		

		an optimization problem.		
Class #	**Chapter Title/Reference Literature**	**Topics to be Covered**	**% of Portion Covered**	
			Individual	**Cumulative**
UNIT-3 Radial-Basis Function Networks				
3Hrs	Text1: Chapters 5 T5.1 to T5.11	Cover's theorem on the separability of patterns, interpolation problem, supervised learning as an ill-posed hypersurface reconstruction problem	23	69
5Hrs		regularization theory, regularization networks, generalized radial-basis function networks		
3Hrs		XOR problem revisited, estimation of the regularization parameter, approximation properties of RBF networks, comparison of RBF networks and multilayer perceptrons; learning strategies.		
UNIT-4 Principal Component Analysis				
6Hrs	Text1:Chapters 8 T8.1 to T8.5	Some intuitive principles of self-organization; principal components analysis;	15	84
4Hrs		Hebbian-based maximum eigen filter; Hebbian-based principal components analysis.		
UNIT-5 Self-Organizing Maps				
4Hrs	Text1: Chapters 9,15 T9.1 to T9.8 T15.1 to T15.8	Feature-mapping models; self-organizing map; properties of the feature map; learning vector quantization	16	100
2Hrs		**Recurrent Networks:** Recurrent network architectures;nonlinear autoregressive with exogenous inputs model;		
3Hrs		Computational power of recurrent networks; learning algorithms; back-propagation through time; real-time recurrent learning. Applications of Neural Networks in Engineering.		

Text Book:

1. S. Haykin, (2003), "Neural Networks: A Comprehensive Foundation", 2nd edition, Prentice Hall of India.

Reference Books:

1. S. Haykin, (2009), "Neural Networks and Learning Machines", 3rd edition, Prentice Hall of India.
2. Alan Murray, (1995), "Applications of Neural Networks", Springer Science+Business Media, New York.
3. T. Hagan, H. B. Demuth and M. Beale, (2002), Neural Network Design, Thomson Learning.

4. M. M. Gupta, L. Jin and N. Homma, (2003), Static and Dynamic Neural Networks: From Fundamentals to Advanced Theory, John Wiley-IEEE Press.