INDEX SHEET

#	Subject code	Subject	Faculty Handling
1	UE20EC201	Mathematics for Electronic Engineers	**Dr. Sanjeev G.** Dr. Raghavendra Kulkarni Dr. Vijaya Krishna A ECC: Prof. Ravi Kumar
2	UE20EC202	Network Analysis and Synthesis	**Dr. Vamsi Krishna** Prof. Sahana Srikanth Prof. Sunil Kumar Prof. Pournamy S. ECC: Dr. Ananya Parameshwaran Prof. Lokesh
3	UE20EC203	Signals and Systems	**Dr. T. S. Chandar** Prof. M. J. Raghavendra Prof. Shwetha R Prof. Shwetha G. ECC: Dr. Ajey S N R Prof. Shreyus
4	UE20EC204	Analog Circuit Design	**Prof. M. S. Sunita** Dr. Kaustav Bhowmick Prof. Sarita Uniyal Dr. Rashmi S B ECC: Prof. Muralidhar Prof. Raghavendra
5	UE20EC205	Computer Aided Digital Design	**Prof. S Santhameena** Prof. B. Rajeshwari Prof. Y. J. Pavithra Prof. Sumanth Sakkara **ECC: Dr. Bajarangbali** Prof. Vinay Reddy
6	UE20EC206	Analog Circuit Design Lab	**Prof. M S Sunitha**
7	UE20EC207	Computer Aided Digital Design Laboratory	**Prof. Santha Meena**

MATHEMATICS FOR ELECTRONICS ENGINEERS (4-0-0-0-4)

Subject Code: UE20EC201 **No. of Hours: 56**

Faculty: SG/ RGK / VKA / Ravi Kumar

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
1	**UNIT-I Complex Analysis** (T1: Chaps. 13-16)	Complex numbers and functions	28.57	28.57
2		Limits, continuity and derivatives		
3		Analytic functions, CR equations (both forms)		
4		Harmonic functions		
5		Line integral in complex plane		
6		Cauchy's integral theorem		
7		Generalization of Cauchy's formula		
8		Taylor's series		
9		Laurent's series		
10		Singularities, poles and residues		
11		Cauchy's residue theorem		
12		Problems session 1		
13		Problems session 2		
14		Problems session 3		
15	**UNIT-II Probability and discrete random variables** (T1: Chap. 24-25)	Basics of probability	14.28	42.85
16		Conditional probability and Bayes' theorem		
17		Independent events		
18		Discrete random variables: Definition		
19		Cumulative distribution function and properties		
20		Probability mass function and density function		
21		Bernoulli and binomial variables		
22		Poisson random variables		
23		Geometric random variables		
24		Problems		
25	**UNIT-III Continuous random variables** (T1: Chap. 24-25, T2: Chap. 3)	Uniform random variable	19.64	62.5
26		Gaussian random variable and properties		
27		Exponential and Rayleigh random variables		
28		Expectation and moments – Continuous and discrete		
29		Moment generating functions and characteristic functions		
30		Transformation of single random variable		
31		Conditional density functions		
32		Problems session 1		
33		Problems session 2		
34		Problems session 3		
35		Problems session 4		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
36	UNIT-IV Multiple random variables (T1: Chap. 24-25, T2: Chap. 5-6)	Joint mass and density functions	21.43	83.93
37		Joint cumulative distributions		
38		Joint MGF and joint CF		
39		Statistical independence		
40		Joint moments: Correlation and covariance		
41		Jacobian transformation		
42		Density of sum of random variables		
43		Central limit theorem		
44		Random vectors and Gaussian distribution		
45		Problems session 1		
46		Problems session 2		
47	UNIT-V Random processes (T1: Chap. 24-25, T2: Chap. 8, 10, 11)	Random processes definition	16.07	100
48		Stationarity and independence		
49		Ergodicity and correlation functions		
50		Power spectral density and properties		
51		Cross PSD and properties		
52		White noise process		
53		Random signal response of linear systems		
54		Spectral characteristics of system response		
55		Spectral factorization		
56		AR, MA and ARMA processes, noise bandwidth		

References:

Book Type	Code	Title & Author	Publication info	
			Publisher	Edition
Text Book 1	T1	Advanced Engineering Mathematics by Erwin Kreyszig	John Wiley and Sons	10
Text Book 2	T2	Probability and Random Processes: With Applications to Signal Processing and Communication by S. Miller and D. Childers	Elsevier India	2

NETWORK ANALYSIS AND SYNTHESIS (4-0-0-0-4)

Subject Code: UE20EC202 **No. of Hours: 56**

Faculty: VK/SHK/SK/PS / Ananya Parameshwaran/Lokesh

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
1	Basic conventions and Analysis: T1 (DC): 8.1 – 8.5, 8.7, 8.8, 8.11, 8.12 T1 (AC): 17.1-17.7 Dot convention and coupled circuits: T1: 21.1, 21.2, 21.8	Reference directions for current and voltage	20	20
2		Independent sources, dependent sources, source conversion		
3		Mesh Analysis: DC circuits and dependent sources		
4		Mesh Analysis: Current sources (super mesh)		
5		Mesh Analysis: AC circuits and dependent sources		
6		Nodal Analysis: DC circuits and floating voltage sources (super node)		
7		Nodal Analysis: AC circuits and floating voltage sources (super node)		
8		Nodal Analysis: Dependent sources (DC and AC)		
9		Bridge networks, Star-delta transformation (DC and AC)		
10		Coupled circuits, Mutual inductance and Dot convention		
11		Mesh analysis of coupled circuits		
12-13	Network theorems: T1 (DC): 9.1 – 9.8 T1 (AC): 18.1 – 18.6	Superposition theorem	18	38
14-15		Thevenin's theorem		
16		Norton's theorem		
17-18		Maximum power transfer theorem		
19-20		Millman's theorem and Introduction to QUCS		
20		Substitution theorem and Reciprocity theorem		
21		Applications of network theorems		
22	Transients: T1 (RC): 10.7 -10.14 T1 (RL): 12.7-12.14 Analysis in s-domain: T2: 6.1-6.3, 6.5, 6.8, 7.1, 7.2	RC transients: Charging phase and discharging phase	22	60
23		RC transients: Initial values and instantaneous values		
24-25		RC transients: Thevenin's equivalent and energy stored by capacitor		
26		RL transients: Storage phase and decay phase		
27		RL transients: Initial values and instantaneous values		
28		RL transients: Thevenin's equivalent and energy stored by inductor		
29-30		Analysis in s-domain: Philosophy of Laplace transform and its properties		
31		Analysis in s-domain: Partial Fraction expansion, Initial value and final value		
32		Analysis in s-domain: Transformed circuit		
33-34		Analysis in s-domain: Application of Thevenin's theorem		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
35	System analysis: T1: 26.1, 26.7-26.9 T2: 9.1, 9. 2, 9.4	Configurations, Two port networks	20	20
36-37		Impedance parameters		
37-38		Admittance parameters		
39-40		Hybrid parameters		
41		ABCD parameters		
42-43		Relation between two port parameters		
44-45		Interconnection of two port networks		
46	Elements of Realizability: T2: 10.1 to 10.4 Synthesis: T2 : 11.1 to 11.5	Elements of realizability: Causality and stability	20	100
47-48		Hurwitz polynomials		
49		Positive real functions		
50		Elementary Synthesis procedures		
51		Properties of LC immitance functions		
52		Synthesis of LC driving point immittances		
53		Properties of R-C impedances and R-L admittances		
54		Synthesis of R-C impedances and R-L admittances		
55		Properties of R-L impedances and R-C admittances		
56		Synthesis of R-L impedances and R-C admittances		

Book Type	Author & Title	Publication information		
		Edition	Publisher	Year
Text book 1	Robert L. Boylestad, *Introductory Circuit Analysis*	Tenth	Prentice Hall	2002
Text book 2	Franklin F Kuo, *Network Analysis and Synthesis*	Second	Wiley India	2006
Ref 1	John O Malley, *Schaum's Outline of Basic Circuit Analysis*	Second	McGraw Hill	1992

SIGNALS AND SYSTEMS (4-0-0-0-4)

Subject Code: UE20EC203 **No. of Hours: 56**

Faculty: TSC/MJ/RS/SWG/ Ajey S N R /Shreyus

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
1-12 (12 hrs)	UNIT-1 Signals and Systems (T1 – Sec. 1.1 – 1.6)	Classification of signals, Continuous-time and discrete-time signals, Transformations of the independent variable, Exponential and sinusoidal signals, The unit impulse and unit step functions, Sa (x) / Sinc functions, Importance of Sinc function, Continuous-time and discrete-time systems, Basic system properties.	19	19
13-22 (10 hrs)	UNIT-II LTI Systems (T1 – Sec. 2.1 – 2.4)	Discrete-time LTI systems: The convolution sum, Continuous-time LTI systems: The convolution integral, Properties of LTI systems, Causal LTI systems described by difference and differential equations (Natural, Forced, and Complete Response).	**19**	**38**
23-34 (12 hrs)	UNIT-III Representation of Periodic (Continuous-time & Discrete-time) signals using Fourierseries. (T1 – Sec. 3.1 – 3.7)	Explanation of Complex Exponentials, Response of LTI systems to complex exponentials, Trigonometric Fourier Series, Fourier series representation of continuous-time periodic signals, Convergence of the Fourier series (brief discussion only),Properties of continuous-time Fourier series (CTFS), Introduction to Fourier series representation of discrete-time periodic signals, Properties of Discrete-time Fourier Series (DTFS).	**19**	**57**
35-46 (12 hrs)	UNIT-IV Continuous-time / Discrete-time Fourier Transform. (T1 – Sec. 4.1 – 4.5, 5.1 – 5.3)	Representation of aperiodic signals: Continuous-time Fourier transform (CTFT), The Fourier transform for periodic signals, Properties of continuous- time Fourier transform, Fourier transform pairs. Discrete-time Fourier transform: Representation of aperiodic signals: the discrete-time Fourier transform (DTFT), The Fourier transform for discrete periodic signals, Properties of discrete-time Fourier transform, Fourier transform pairs, Duality. Introduction to Sampling: Sampling theorem, Nyquist Criterion.	**23**	**80**
47-56 (10 hrs)	UNIT-V Z-Transforms (T1 – 10.1 – 10.3, 10.5 – 10.7, 10.9)	The Z-transform, The region of convergence (ROC) for the Z-transform, The inverse Z-transform, Properties of the Z-transform, Z-transform pairs, Analysis and characterization of LTI systems using Z-transforms. The unilateral Z-transform and solution of difference equations.	**20**	**100**

References:

Book Type	Code	Title & Author	Publication Info		
			Edition	Publisher	Year
Textbook - 1	T1	"Signals and Systems" Alan V Oppenheim, Alan S. Willsky	2nd	Pearson Education Asia	2013
Reference Book - 1	R1	"Signals and Systems" Simon Haykin & Barry Van Veen	2nd	John Wiley & Sons	2004
Reference Book - 2	R2	"Signals Processing and Linear Systems" B.P. Lathi	1st	Ind Press	2006
Reference Book - 3	R3	"Analog and Digital Signal Processing"Ashok Ambardar	2nd	Thomas Learning	1999
Reference Book – 4	R4	"Signals and Systems" S. K. Mitra	1st	Oxford Univ. Press	2016

ANALOG CIRCUIT DESIGN (4-0-0-0-4)

Subject Code: UE20EC204 **No. of Hours: 56**

Faculty: MSS/KB/SU/SBR/Muralidhar/Raghavendra

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
1	**Unit I - Physics of MOS transistor T1: Chapter2**	MOSFET Structure	18	18
2		MOS Symbols, MOS I/V characteristics		
3				
4-5		Derivation of I/V characteristics		
6		MOS transconductance		
7		Second -order effects		
8		MOS Device Capacitances		
9		MOS Small – signal model		
10		MOS Spice model, NMOS versus PMOS		
11	**Unit II – CMOS Amplifiers T1: Chapter 3**	General Considerations	21	39
12-13		CS stage with resistive load		
14-15		CS stage with diode-connected load		
16		CS stage with current- source load		
17		CS stage with source degeneration		
18-19		Source Follower		
20-21		CG Amplifier		
22		Cascode stage		
23	**Unit III- CMOS Current Mirrors and Differential Amplifier T1: Chapters 4 and 5**	Basic current mirrors	22	61
24-25		Cascode current mirrors		
26		Single -ended and differential operation		
27		Basic Differential pair		
28		Qualitative Analysis		
29		Small – signal Analysis		
30-31		Common – mode Response		
32		Differential pair with MOSFET load		
33-34		Differential pair with active load – Small signal analysis		
35	**Unit IV - Frequency Response and Feedback Amplifiers T1: Chapters 6 and 8**	Miller effect	21	82
36-38		Frequency Response of CS amplifier		
39		Feedback – General Considerations		
40-41		Properties of negative feedback		
42-43		Types of amplifiers		
44-46		Feedback topologies		

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
47-48	**Unit V - Bipolar Amplifiers and Power Amplifiers T2: Chapters 5 and 14**	Bipolar Amplifiers – General Considerations	18	100
49-50		Operating point – Analysis and Design		
51-52		Bipolar Amplifier Topologies – Common Emitter Topology		
53		Power Amplifiers – General Considerations		
54		Emitter – Follower as Power Amplifier		
55		Push – pull stage		
56		Improved push -pull stage		

Text Books:

1) Behzad Razavi, *"Design of Analog CMOS Integrated Circuits"*, McGraw Hill, 2nd Edition, 2017.
2) Behzad Razavi, "Fundamentals of Microelectronics", TMH Publisher, 2nd Edition, 2013.

Reference Books:

1) Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University, 2nd Edition, 2002.
2) Sedra and Smith, "Microelectronic Circuits: Theory and Applications", 7th edition, 2017.

COMPUTER AIDED DIGITAL DESIGN (4-0-0-0-4)

Subject Code: UE20EC205 **No. of Hours: 56**

Faculty: SSM / BR/ YJP/SS/Bajarangbali/Vinay Reddy

Class #	Chapter Title/Reference Literature	Topics to be Covered	% of Portion Covered	
			Reference chapter	Cumulative
Unit 1: Number System & Logic Gates:				
1	1.2.1	Levels of abstraction for an electronic computing system, Fig 1.1	1	1
2-3	1.4	Number System	4	5
4-5	1.5	Logic Gates	3	8
6-7	2.2	Boolean Equations	4	12
8-9	2.3	Boolean Algebra	4	16
10	2.4	From Logic to Gates	2	18
Unit 2: Combinational Logic Design:				
11	2.1	Introduction	1	19
12	2.5	Multilevel Combinational Logic	2	21
13	2.6	X's and Z's	2	23
14-15	2.7	Karnaugh Maps	3	26
16	2.8	Combinational Building Blocks	2	28
17	2.9	Timing	2	30
18	4.1	HDL : Introduction	2	32
19-20	4.2	Combinational Logic	2	34
21	4.3	Structural Modeling	3	37
22	4.7.1	Data Types	2	39
Unit 3: Sequential Logic Design:				
23	3.1	Introduction	2	41
24-26	3.2	Latches & Flip Flops	5	46
27-28	3.3	Synchronous Logic Design	3	49
29-30	3.4	Finite State Machines	4	53
31-33	3.5	Timing of Sequential Logic	5	58
34	3.6	Parallelism	2	60
Unit 4: Hardware Description Language 2:				
35-37	4.4	Sequential Logic	5	65
38-40	4.5	More Combinational Logic	5	70
41-42	4.6	Finite State Machines	4	74
43-44	4.8	Parameterized Modules	4	78
45-46	4.9	Testbenches	4	82
Unit 5: Digital Building Blocks:				
47-49	5. 1 & 5.2	Introduction, Arithmetic Circuits	5	87
50	5.3	Number Systems	2	89
51	5.4	Sequential Building Blocks	2	91
52-54	5.5	Memory Arrays	5	96
55-56	5.6	Logic Arrays	4	100

Text Book:

1. David Money Harris and Sarah L Harris, "Digital Design and Computer Architecture", Elsevier, 2nd Edition, 2019.

ANALOG CIRCUIT DESIGN LABORATORY (0-0-2-1-1)

Subject Code: UE20EC206 **No. of Weeks : 13**

Faculty: MSS

Week No.	Expt. No.	Experiment
1.	1.	Diode applications: Clipping and Clamping
2.	2.	Biasing BJT and CE Amplifier (Voltage divider biasing)
3.	3.	Push pull Power amplifier using BJT
4.	4.	Single stage CS amplifier
5.	-	Repetition class for Hardware expts (Expts. 1 -4)
6.	5.	Introduction to Mentor Graphics tool, MOSFET Characteristics
7.	-	Theory ISA – 1.
8.	6.	CS Amplifier with different loads
9.	7.	Source follower and Cascode
10.	8 & 9	Current Mirror and Differential Amplifier
11.	-	Break.
12.	10.	Feedback Amplifier
13.	-	FSA for Lab courses
14.	-	Theory ISA - 2
15.	-	Final Repetition class

COMPUTER AIDED DIGITAL DESIGN LABORATORY (0-0-2-1-1)

Subject Code: UE20EC207
Faculty: SSM

Course Description:

This laboratory course is intended to expose students to design digital circuits and its applications using the state of art ASIC/FPGA tools. This course includes simulation and implementation of combinational and sequential circuits. SystemVerilog HDL is used to programme the FPGA devices and to design the FSM based systems.

Course Objectives:

- The Verilog RTL code of Digital System functionality is verified using Xilinx Vivado Simulator
- The Verilog RTL code of Digital System functionality is synthesized and implemented on Artix7/Basys 3/Intel DE-series FPGA boards**.**

Course Outcomes:

Students completing the course should be able to

- Write synthesizable RTL SystemVerilog Code and perform behavioural verification using test vectors.
- Program on Artix-7 FPGA and perform testing for functionality.
- Understand FPGA flow using Xilinx Vivado tool/Intel Quartus Prime Design Software.

Course Content:

Cycle-1

- Introduction to Tool – Simulation and Synthesis Flow using Logic gates HDL Program.
- Combinational Logic Design – Multiplexers/Encoders/Decoders Design.
- Combinational Logic Design - Adders Design & Conversions (Binary to Decimal Conversion).
- Sequential Logic Design – Latches & Flip Flops.
- Sequential Logic Design – Counters Designs.

Cycle-2

- Implementation of an 8-bit accumulator.
- Implementation of an 8 x 8 multiplier circuit.
- Implementation of FSM Designs.
- Implementation of Sequence detectors (Mealy Model & Moore Model)
- Design of Memory blocks.

https://software.intel.com/content/www/us/en/develop/topics/fpga-academic/materials-digital-logic.html